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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/517,591 | 12/13/2004 | Hideki Osaka | 520.44478X00 | 1819 |

20457 7590 02/08/2007

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| EXAMINER | |
|---|---|
| CLEARY, THOMAS J | |
| ART UNIT | PAPER NUMBER |
| 2111 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 02/08/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/517,591 | OSAKA, HIDEKI | |
| | Examiner | Art Unit | |
| | Thomas J. Cleary | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 13 December 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 13 December 2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Acknowledgment is made of Applicant's claim for foreign priority based on an application filed in Japan on 1 July 2002. It is noted, however, that applicant has not filed a certified copy of the Japanese application as required by 35 U.S.C. 119(b).

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1-18 recite the limitation "the wirings are each connected to a second semiconductor device". Neither the specification nor the drawings support the wirings each connected to a second semiconductor device. The specifications and drawings appear to disclose that the wirings are each connected to respective

separate semiconductor devices. Claim 11 recites the limitation "a wiring extending from the second semiconductors is folded within the motherboard". Neither the specification nor the drawings support folding a wiring extending from the second semiconductors within the motherboard. Claims 15-18 recite the limitation "a driver that outputs a signal reversing the output data...". Neither the specification nor the drawings support the output data being reversed.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

5. Claims 6, 7, 9, 10, 15, 16, 17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. It is unclear if the aforementioned claims are intended in import limitations from the parent claims, as limitations from the parent claims appear to be excluded.

6. Claims 2-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 2-13 recite the limitation "when it is assumed that..." at multiple locations. It is unclear as to the metes and bounds of the claim limitations, as they presuppose a hypothetical situation.

7. Claims 4-5 and 7-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 4-5 and 7-13 recite the limitation "the degree of coupling". There is insufficient antecedent basis for this limitation in the claim. It is unclear what a degree of coupling is, nor how it is changed by satisfying $w1 \geq w2 \geq w3 \geq \ldots \geq wn$.

8. Claims 5 and 7-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 5 and 7-12 recite the limitation "the i-th directional coupler has the degree of coupling Kbi given by $Kbi = Kbi * (1 + (i - 1) * x)$, where the degree of coupling Kb1 of the first directional coupler has a coefficient of $x = 0.1$ to 0.2". It is unclear what the value of x is in the equation for Kbi, as x is only defined for Kb1. Further, the only values of i and x for which the equation given would be valid is for $i = 1$ or $x = 0$, which would result in the parenthetical portion of the equation being equal to 1, and thus $Kbi = Kbi * 1$. Any other value for the parenthetical portion of the equation would result in an invalid equation. Further, this equation is not supported in the specification.

9. Claims 3, 6, 8, 11, and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 3, 6, 8, 11, and

12 recite the limitation "a difference among the coupling lengths of L1, L2, L3, and L4 is within 10 mm.". It is unclear if the difference is the total difference between the shortest (L1) and the longest (L4) or if it is the difference between adjacent coupling lengths (L1-L2, L2-L3, or L3-L4).

10. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 7 recites the limitation "the wiring interval". There is insufficient antecedent basis for this limitation in the claim.

11. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 10 recites the limitation "the memory controller". There is insufficient antecedent basis for this limitation in the claim.

12. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 11 recites the limitations "a plurality of second semiconductors are mounted on a plurality of daughter boards" and "a wiring extending from the second semiconductors is folded within the motherboard". It is unclear how a wiring which extends from a second semiconductor which is on a daughter board can be folded within the motherboard.

13. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 12 recites the limitations "the wiring extending from the second semiconductor"; "the folded main line"; and "the sub coupling wirings". There is insufficient antecedent basis for these limitation in the claim.

14. Claims 14-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 14-18 recite the limitation "a signal having a reverse polarity to the data signal is again inputted to the directional couplers...". It is unclear how this signal can be again inputted to the directional couplers, as the signal was not previously inputted.

15. Claims 14-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 14-18 recite the limitation "a signal...is again inputted to the directional couplers with an amplitude that is 10 to 20% of the amplitude of the drive pulse after a reciprocating delay time of the directional couplers". It is unclear if the amplitude is 10 to 20% of the initial amplitude

of the drive pulse, or if the signal is 10 to 20% of the current amplitude of the drive pulse after a reciprocating delay time.

16. The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

17. Claims 6, 7, 9, 10, 15, 16, 17, and 18 are rejected under 35 U.S.C. 112, fourth paragraph, for failing to further limit the parent claim. The aforementioned claims clearly seek to exclude the limitations of the claims from which they respectively depend. It appears that Applicant intends to claim a printed circuit board (Claims 6 and 7), a memory module (Claims 9, 10, and 18), a semiconductor device (Claim 15), a main controller (Claim 16), and a memory (Claim 17), which can be used in the bus system of the parent claims. If this is the case, Applicants should present the claims in independent format restating the system within which the printed circuit board, memory module, semiconductor device, main controller, or memory operates such as in a Jepson-style format.

***Claim Rejections - 35 USC § 101***

18. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

19. Claims 2, 3, 6, 8, 10, 11, 12, and 13 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. Claim 1 recites the limitation of "each of the directional couplers has a different coupling length...". Claims 2, 3, 5, 8, 10, 11, 12, and 13 recite the limitation of "L1 ≤ L2 ≤ L3 ≤ ... ≤ Ln". Thus, the claims encompass the situation when any or all of L1 – Ln are equal, which directly contradicts the limitation of each of the couplers having a different length.

***Claim Rejections - 35 USC § 102***

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the Applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the Applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

21. Claims 1-4, 6-10, and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 6,111,476 to Williamson ("Williamson").

22. In reference to Claim 1, Williamson discloses a bus system (See Figure 1 Number 24) that transfers data between a plurality of semiconductor devices (See Figure 1 Numbers 22 and 34), wherein: a first wiring is drawn out of a first semiconductor (See Figure 1 Numbers 22 and 24), a plurality of wirings are arranged in parallel with the first wiring to constitute directional couplers (See Figure 1 Number 32), and the wirings are each connected to a second semiconductor device (See Figure 1 Number 34); and each of the directional couplers has a different coupling length so that signal amplitudes generated by the plurality of directional couplers may be substantially the same (See Figure 1; Column 1 Line 52 – Column 2 Line 3; and Column 3 Lines 42-53).

23. In reference to Claim 2, Williamson discloses the limitations as applied to Claim 1 above. Williamson further discloses that when lengths of n directional couplers connected are L1, L2, L3, ... Ln in the order nearer to the first semiconductor, generated signal amounts of the directional couplers are substantially the same by satisfying $L1 \leq L2 \leq L3 \leq \ldots \leq Ln$ (See Column 3 Lines 42-53).

24. In reference to Claim 3, Williamson discloses the limitations as applied to Claim 2 above. Williamson further discloses that when the second semiconductor comprises four second semiconductors, and lengths of the directional couplers are L1, L2, L3 and L4 in the order nearer to the first semiconductor, a difference among

the coupling lengths of L1, L2, L3 and L4 is within 10 mm (See Column 4 Lines 54-57).

25. In reference to Claim 4, Williamson discloses the limitations as applied to Claim 1 above. Williamson further discloses that when intervals between two parallel lines that constitute n directional couplers connected are w1, w2, w3, ... wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying w1 = w2 = w3 = ... = wn, and generated signal amounts of the directional couplers are substantially the same (See Figure 1).

26. In reference to Claim 6, Williamson discloses the limitations as applied to Claims 2 and 3 above. Williamson further discloses a printed circuit board wherein the directional couplers have the coupling lengths that satisfy $L1 \leq L2 \leq L3 \leq \ldots \leq Ln$ (See Column 1 Lines 12-20 and Column 3 Lines 42-53).

27. In reference to Claim 7, Williamson discloses the limitations as applied to Claim 4 above. Williamson further discloses a printed circuit board wherein the directional couplers are provided which have the wiring intervals that satisfy w1 = w2 = w3 = ... = wn (See Column 1 Lines 12-20 and Figure 1).

28. In reference to Claim 8, Williamson discloses the limitations as applied to Claims 2, 3, and 4 above. Williamson further discloses that the first semiconductor

and the directional couplers are mounted on a motherboard; a plurality of the second semiconductors are mounted on a plurality of daughter boards; the plurality of daughter boards are connected to the motherboard through connectors; and intervals of the plurality of daughter boards are constant independently from the lengths of the directional couplers (See Figure 1 and Column 1 Lines 12-20).

29. In reference to Claim 9, Williamson discloses the limitations as applied to Claim 4 above. Williamson further discloses a memory module, wherein a plurality of memories are mounted instead of the plurality of second semiconductors, directional couplers used for signal transmission between the first semiconductor and the memories are disposed within the memory module, and the memories are arranged at regular intervals within the memory module (See Column 1 Lines 12-15); and when two parallel lines that constitute n directional couplers connected to the bus system are w1, w2, w3, ... wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying w1 = w2 = w3 = ... = wn, and generated signal amounts of the directional couplers are substantially the same (See Figure 1).

30. In reference to Claim 10, Williamson discloses the limitations as applied to Claim 9 above. Williamson further discloses that a data signal is transferred through a data signal bus by using directional couplers disposed within a motherboard, and a control signal is transferred through a control signal bus by using directional couplers

disposed within a daughter board (See Column 1 Lines 12-15); when the lengths of the directional couplers in each of n memory modules are L1, L2, L3 and L4 in the order nearer to the memory controller, L1 ≤ L2 ≤ L3 ≤ ... ≤ Ln is satisfied (See Column 3 Lines 42-53); when the intervals between two parallel lines that constitute n directional couplers connected to the control signal bus are w1, w2, w3, ... wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying w1 = w2 = w3 = ... = wn, and generated signal amounts of the directional couplers are substantially the same in all memories (See Figure 1).

31. In reference to Claim 13, Williamson discloses the limitations as applied to Claims 2 and 4 above. Williamson further discloses that when the lengths of the directional couplers connected to the bus system are L1, L2, L3 and L4 in the order nearer to the first semiconductor, L1 ≤ L2 ≤ L3 ≤ ... ≤ Ln is satisfied (See Column 3 Lines 42-53); and when the intervals between two parallel lines that constitute n directional couplers connected to the bus system are w1, w2, w3, ... wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying w1 = w2 = w3 = ... = wn, and generated signal amounts of the directional couplers are substantially the same (See Figure 1).

32. In reference to Claim 14, Williamson discloses a bus system (See Figure 1 Number 24) that transfers data between a plurality of semiconductor devices (See

Figure 1 Numbers 22 and 34), wherein: a first wiring is drawn out of a first semiconductor (See Figure 1 Numbers 22 and 24), a plurality of wirings are arranged in parallel with the first wiring to constitute directional couplers (See Figure 1 Number 32), and the wirings are each connected to a second semiconductor device (See Figure 1 Number 34); and each of the directional couplers has a different coupling length so that signal amplitudes generated by the plurality of directional couplers may be substantially the same (See Figure 1; Column 1 Line 52 – Column 2 Line 3; and Column 3 Lines 42-53) and a drive pulse corresponding to a transmitted data signal is inputted to the directional couplers, a signal having a reverse polarity to the data signal is again inputted to the directional couplers with an amplitude that is 10 to 20% of the amplitude of the drive pulse after a reciprocating delay time of the directional couplers, and the signal having the reverse polarity continues until subsequent data is received (See Column 3 Lines 54-65).

33. Claims 1-2, 4, 6-8, and 13-14are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 7,126,437 to Simon et al. ("Simon").

34. In reference to Claim 1, Simon discloses a bus system (See Figure 1 Number 10) that transfers data between a plurality of semiconductor devices (See Figure 1 Numbers 24, 26, 28, and 30), wherein: a first wiring is drawn out of a first semiconductor (See Figure 1 Number 10 and Figure 3), a plurality of wirings are arranged in parallel with the first wiring to constitute directional couplers (See Figure

1 Numbers 12, 14, and 16 and Figure 3), and the wirings are each connected to a second semiconductor device (See Figure 1 Numbers 24, 26, and 28 and Figure 3); and each of the directional couplers has a different coupling length so that signal amplitudes generated by the plurality of directional couplers may be substantially the same (See Figure 3 and Column 2 Lines 14-25).

35. In reference to Claim 2, Simon discloses the limitations as applied to Claim 1 above. Simon further discloses that when lengths of n directional couplers connected are L1, L2, L3, ... Ln in the order nearer to the first semiconductor, generated signal amounts of the directional couplers are substantially the same by satisfying $L1 \leq L2 \leq L3 \leq \ldots \leq Ln$ (See Figure 3 and Column 2 Lines 2-25).

36. In reference to Claim 4, Simon discloses the limitations as applied to Claim 1 above. Simon further discloses that when intervals between two parallel lines that constitute n directional couplers connected are w1, w2, w3, ... wn in the order nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying $w1 = w2 = w3 = \ldots = wn$, and generated signal amounts of the directional couplers are substantially the same (See Figure 5 and Column 3 Lines 17-20).

37. In reference to Claim 6, Simon discloses the limitations as applied to Claim 2 above. Simon further discloses a printed circuit board wherein the directional

couplers have the coupling lengths that satisfy L1 ≤ L2 ≤ L3 ≤ ... ≤ Ln (See Figure 3; Column 2 Lines 2-25; and Column 3 Lines 10-16).

38. In reference to Claim 7, Simon discloses the limitations as applied to Claim 4 above. Simon further discloses a printed circuit board wherein the directional couplers are provided which have the wiring intervals that satisfy w1 = w2 = w3 = ... = wn (See Figure 5; Column 3 Lines 17-20; and Column 3 Lines 10-16).

39. In reference to Claim 8, Simon discloses the limitations as applied to Claims 2 and 4 above. Simon further discloses that the first semiconductor and the directional couplers are mounted on a motherboard; a plurality of the second semiconductors are mounted on a plurality of daughter boards; the plurality of daughter boards are connected to the motherboard through connectors; and intervals of the plurality of daughter boards are constant independently from the lengths of the directional couplers (See Figure 5 and Column 3 Lines 10-16).

40. In reference to Claim 13, Simon discloses the limitations as applied to Claims 2 and 4 above. Simon further discloses that when the lengths of the directional couplers connected to the bus system are L1, L2, L3 and L4 in the order nearer to the first semiconductor, L1 ≤ L2 ≤ L3 ≤ ... ≤ Ln is satisfied (See Figure 3 and Column 2 Lines 2-25); and when the intervals between two parallel lines that constitute n directional couplers connected to the bus system are w1, w2, w3, ... wn in the order

nearer to the first semiconductor, the degrees of coupling of the directional couplers are changed by satisfying w1 = w2 = w3 = ... = wn, and generated signal amounts of the directional couplers are substantially the same (See Figure 5 and Column 3 Lines 17-20).

41. In reference to Claim 14, Simon discloses a bus system (See Figure 1 Number 10) that transfers data between a plurality of semiconductor devices (See Figure 1 Numbers 24, 26, 28, and 30), wherein: a first wiring is drawn out of a first semiconductor (See Figure 1 Number 10 and Figure 3), a plurality of wirings are arranged in parallel with the first wiring to constitute directional couplers (See Figure 1 Numbers 12, 14, and 16 and Figure 3), and the wirings are each connected to a second semiconductor device (See Figure 1 Numbers 24, 26, and 28 and Figure 3); and each of the directional couplers has a different coupling length so that signal amplitudes generated by the plurality of directional couplers may be substantially the same (See Figure 3 and Column 2 Lines 14-25) and a drive pulse corresponding to a transmitted data signal is inputted to the directional couplers, a signal having a reverse polarity to the data signal is again inputted to the directional couplers with an amplitude that is 10 to 20% of the amplitude of the drive pulse after a reciprocating delay time of the directional couplers, and the signal having the reverse polarity continues until subsequent data is received (See Column 1 Line 63 – Column 2 Line 12).

42. Claims 14-18 recite the limitation "a signal having a reverse polarity to the data signal is again inputted to the directional couplers with an amplitude that is 10 to 20% of the amplitude of the drive pulse after a reciprocating delay time...". In light of the specification and the drawings (See Figure 15A), the Examiner will interpret this to mean that the signal is driven to an amplitude that is 10 to 20% less than the amplitude of the drive pulse. If this interpretation is incorrect, Applicant is advised to amend the Claim language to clearly claim the intended interpretation and provide arguments commensurate with the enablement provided by the specification and the drawings explaining the correct interpretation.

***Conclusion***

43. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: "Empirical Relations for Capacitive and Inductive Coupling Coefficients of Coupled Microstrip Lines" by Kal et al.; "When are Transmission-Line Effects Important for On-Chip Interconnections?" by Deutsch et al.; "Capacitive Coupling Solves the Known Good Die Problem" by Salzman et al.; "Manufacturability of Capacitively Coupled Multichip Modules" by Knight, Jr. et al.; "An Alignment Insensitive Separable Electromagnetic Coupler for High Speed Digital Multidrop Bus Applications" by Benham et al.; "Application of Capacitive Coupling to Switch Fabrics" by Salzman et al.; US Patent Number 7,088,198 to Simon et al.; US Patent Number 7,075,795 to Wu et al.; US Patent Number 6,882,239 to Miller et al.;

US Patent Number 6,745,268 to Greeff et al.; US Patent Number 6,697,420 to Simon et al.; US Patent Number 6,496,889 to Perino et al.; US Patent Number 5,365,205 to Wong; US Patent Number 3,786,418 to Nick; US Patent Number 3,764,941 to Nick; US Patent Number 3,619,504 to DeVeer et al.; US Patent Number 3,516,065 to Bolt et al.; US Patent Number 5,329,263 to Manami; US Patent Number 5,376,904 to Wong; and US Patent Number 6,414,891 to Kuge et al.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJC

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